REMARKS

Claims 1, 3-5 and 7-12 are pending in the application. Claims 1, 3, 9, 11 and 12 have been amended. Claims 2, 6, 13 and 14 have been canceled. Applicants submit that no new matter has been added to the application by the Amendment.

Applicants respectfully request that the Amendment After Final be entered in accordance with 37 CFR §116 and MPEP 714.13 since the Amendment places the application in condition for allowance.

Rejection - 35 U.S.C. § 102

The Examiner rejected claims 1-3, 12 and 13 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,661,294 (Terashima et al.).

Claims 1 and 12 have been amended so that each recite a PLL clock generator comprising a frequency divider, a phase comparator, a time width detector and a phase shifter. The amendment is supported at least at paragraphs [0050] – [0054] of the application.

The present invention is directed to achieving a phase locked condition more rapidly than does a conventional PLL while minimizing jitter. In the PLL clock generator circuit, the frequency divider counts a clock signal and divides the frequency of the clock signal by N so as to output a frequency-divided clock signal. The phase comparator detects a phase difference between the input signal and the output signal of the frequency divider. The time width detector outputs a positive phase difference signal and a negative phase difference signal based on the phase difference signal. The phase shifter advances the count of the frequency divider if the amplitude of the positive phase difference signal is equal to or greater than a first predetermined value and delays the count of the frequency divider if the amplitude of the negative phase difference signal is equal to or greater than a second predetermined value so as to change the phase of the output signal of the frequency divider.

Terashima et al. is directed to stabilizing the phase of a PLL clock output during an abnormal condition such as when the input clock signal is interrupted. Terashima et al. uses an abnormal condition detecting unit 10 to detect when the pulse width of the phase error signal Sc exceeds a predetermined value. Upon detecting the abnormal condition, the abnormal conditioning unit 10 outputs a signal Sm to the control unit 11 which, in turn, outputs a signal Si to the phase difference holding unit 2 to hold the phase error signal Sc output from the phase

comparing unit 1 (column 9, lines 6-27). The control unit also controls the selecting unit to select the output Sf from the phase difference holding unit 2.

When the abnormal condition ends, the control unit 11, outputs the control signal Si to the frequency divider 12 to synchronize the output Sb of the phase detector 12 to the phase of the external clock signal Sa and to select the output of the phase comparing unit Sc.

Terashima et al. differs from claims 1 and 12 in the following respects:

1. The abnormal detecting unit 10, while detecting whether an abnormal condition exists merely outputs a control signal that indicates whether or not the width of the phase error signal is less than a predetermined threshold. In contrast, the claimed time width detector outputs a positive phase difference signal and a negative phase difference signal.

2. In the process of relocking the PLL to the external clock, the PLL described by Terashima et al. merely provides a pulse from the control unit 11 to the frequency divider 12 to force the phase of the frequency divider output signal Sb to be in phase with the external clock signal Sa (see col. 9, lines 54-58 and Fig. 2E), irrespective of whether the phase of the frequency divider output signal is advanced or retarded. In contrast, the claims 1 and 12 each recite a phase shifter for advancing/retarding the count of the frequency divider based on the amplitude of the positive/negative phase difference signals.

The PLL of Terashima et al is different from the present invention. Terashima et al. relocks the PLL by jamming the phase of the frequency divider to the phase external clock signal. In contrast, the present invention utilizes the time width detector determine whether the phase of the frequency divider should be advanced or retarded and a phase shifter to control the advancing and retarding of the frequency divider.

Terashima et al. does not include a time width detector or a phase shifter equivalent to either the claimed time width detector or the phase shifter. Accordingly, Applicants respectfully request reconsideration and withdrawal of the 102 rejection of claims 1 and 12.

Further, it is respectfully submitted that since claim 1 has been shown to be allowable, claims 2-3 dependent on claim 1 are allowable, at least by their dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims 2-3.

Rejection - 35 U.S.C. § 103

The Examiner rejected claims 7, 9, 10 and 11 under 35 U.S.C. § 103(a) as being unpatentable over Terashima et al. and further in view of the acknowledged prior art of Figure 7 in this application.

Amended claims 9 and 11 each recite a time width detector and a phase shifter. The admitted prior art does not teach or suggest either a time width detector or a phase shifter. Accordingly, claims 9 and 11 are allowable for the same reasons that claims 1 and 12 are allowable.

Claim 7 depends from allowable claim 1. Claim 10 depends from allowable claim 9. Accordingly, claims 7 and 10 are allowable, at least by their dependency.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 7, 9, 10 and 11.

The Examiner rejected claims 4 and 5 under 35 U.S.C. § 103(a) as being unpatentable over Terashima et al. in view of U.S. Publication 2004/0027940 (Minamino et al.) U.S. Publication 2003/0002406 (Deguchi) or U.S. Patent No. 7,012,865 (Deguchi).

Claims 4 and 5 depend from allowable claim 1. Neither U.S. Publication 2004/0027940 (Minamino et al.), U.S. Publication 2003/0002406 (Deguchi) nor U.S. Patent No. 7,012,865 (Deguchi) each or suggest either a time width detector or a phase shifter. Accordingly, claims 4 and 5 are allowable, at least by their dependency. Accordingly, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 4 and 5.

The Examiner rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Terashima et al. in view of U.S. Publication 2004/0027940 (Minamino et al.) U.S. Publication 2003/0002406 (Deguchi) or U.S. Patent No. 7,012,865 (Deguchi) and further in view of admitted prior art.

Claim 8 depends from allowable claim 1. Neither U.S. Publication 2004/0027940 (Minamino et al.), U.S. Publication 2003/0002406 (Deguchi) or U.S. Patent No. 7,012,865 (Deguchi) or the admitted prior art teach or suggest either a time width detector or a phase

shifter. Accordingly, claim 8 is allowable, at least by its dependency. Accordingly, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claim 8.

Conclusion

Insofar as the Examiner's rejections to claims 1-5 and 7-14 have been fully addressed, the instant application is in condition for allowance. Withdrawal of the Final Rejection, formal entry of the present "Amendment After Final," and issuance of a Notice of Allowability is therefore earnestly solicited.

Respectfully submitted,

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